UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,096	03/01/2004	Errol Todd Ryan	0180367	2466

25700 7590 06/09/2009

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
LEBENTRITT, MICHAEL	
ART UNIT	PAPER NUMBER
2829	
MAIL DATE	DELIVERY MODE
06/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,096	RYAN ET AL.	
	Examiner	Art Unit	
	MICHAEL S. LEBENTRITT	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9-12,14-17 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,14-17 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

Claims 1, 2, 4-7, 9-12, 14-17, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and in further View of Tseng (US 2005/0035460).

Regarding claim 1, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (200 in Fig. 2D); forming a gate dielectric on the semiconductor substrate (206 in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (208 in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (210 in Fig. 2D; column 3, line 59- column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10) with uniform a thermal budget having a temperature dependent upon a silicide metal (the instant application on p. 9, lines 23-24 discloses that the thermal budget for nickel silicides is about 400 °C to 450 °C; Chang discloses forming the silicide at a temperature of about 400 to 800 °C, overlapping with the entirety of the thermal budget of nickel silicides).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes with uniform the thermal budget for forming the silicide; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Lim teaches depositing an interlayer dielectric having contact holes

(paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact holes with uniform the thermal budget for forming the silicide (tungsten nitride, paragraph 0021; Lim discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 2, Chang and Lim together teach the method of claim 1. Lim further teaches that forming the contact liners uses an atomic layer deposition process (paragraph 0021).

Regarding claim 4, Chang and Lim together teach the method of claims 1 and 11. Chang further teaches that forming the silicide forms a nickel silicide (column 4, line 56- column 5, line 10).

Regarding claim 4, Chang and Lim together teach the method of claims 1 and

11. Chang further teaches that forming the silicide forms a nickel silicide (column 4, line 56- column 5, line 10).

Regarding claim 6, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (200 in Fig. 2D); forming a gate dielectric on the semiconductor substrate (206 in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (208 in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (210 in Fig. 2D; column 3, line 59- column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10) within uniform a thermal budget having a temperature of less than about 400 degrees centigrade (Chang teaches forming the silicide at a temperature of about 400 °C to 800 °C, which overlaps with the claimed temperature range at about 400 °C, and since the claimed temperature range "less than about 400 degrees centigrade" is not specific, it could be interpreted as, for example, "less than 402 degrees centigrade," which Chang teaches).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes with uniform the thermal budget for forming the nickel silicide; and forming tungsten contacts in the contact holes over the contact liners.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes (paragraph 0021) with uniform the thermal budget for forming the silicide (Lin discloses keeping the reaction chamber at a temperature

between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming tungsten contacts in the contact holes over the contact liners (paragraph 0026).

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes (paragraph 0021) within uniform the thermal budget for forming the silicide (Lin discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming tungsten contacts in the contact holes over the contact liners (paragraph 0026).

Regarding claim 7, Chang and Lim together teach the method of claim 6. Lim further teaches that forming the tungsten nitride liners uses an atomic layer deposition process (paragraph 0021).

Regarding claims 1, 4, 6, 9, 11, 12, and 17, 23 Chang and Lim together teach the method (note 35 U.S.C. 103(a) rejection above), but do not teach that forming the nickel silicide uses an ultra-uniform silicide having approximately less than 3% variation in thickness on the source/drain junctions. Tseng teaches forming nickel silicide layers with a thickness of 50 - 350 /~ (paragraph 0037), with uniform the limits indicated in the instant specification on page 8, line 4 of "not more than 50 ,/k thickness." Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-

uniform, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009). In regards Chang and Lim not teaching forming an ultra forming an ultra-uniform silicide having approximately less than 3% variation in thickness on the source/drain junctions. The variation in thickness would be determined through routine experimentation and would not lend itself to patentability in the instant application without showing unexpected results. See in Re Aller.

Regarding claim 11, Chang teaches an integrated circuit comprising a semiconductor substrate (200 in Fig. 2D); a gate dielectric on the semiconductor substrate (206 in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (208 in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (210 in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; contact liners in the contact holes; and contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts. Chang also does not teach that the silicide is an ultra- uniform silicide having approximately less than 3% variation in thickness on the source/drain junctions.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph :

0020) therein above a semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 - 350/~, (paragraph 0037), with uniform the limits indicated in the instant specification on page 8, line 4 of "not more than 50 A thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-uniform, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 12, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Chang further teaches that the silicide is a nickel silicide (column 4, line 56 - column 5, line 10).

Regarding claim 15, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts in the contact holes are tungsten (paragraph 0026).

Regarding claim 16, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts are a tungsten material (paragraph 0026) and the contact liners are a tungsten nitride material (paragraph 0021).

Regarding claim 17, Chang teaches an integrated circuit comprising a semiconductor substrate (200 in Fig. 2D); a gate dielectric on the semiconductor substrate (206 in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (208 in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (210 in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; tungsten nitride contact liners in the contact holes; and tungsten contacts in the contact holes over the contact liners. Chang also does not teach that the silicide is an ultra-uniform silicide having approximately less than 3% variation in thickness on the source/drain junctions.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners (tungsten, paragraph 0026). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 - 350 A (paragraph 0037), within uniform the limits indicated in the instant specification on page 8, line 4 of "not more than 50 A thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-uniform silicide having approximately less than 3% variation in thickness on the source/drain junctions, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 20, Chang, Lim, and Tseng together teach the method of claim

17. Chang further teaches that the gate and source and drain regions are ion-implanted with arsenic prior to the formation of nickel silicide on the gate and source and drain regions, so the nickel silicide further comprises arsenic doping (column 4, lines 23-39).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claims 6 above, and further in view of Tseng (U.S. 2005/0035460) and Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1).

Regarding claim 10, Chang and Lim together teach the method of claim 6 (note 35 U.S.C. 103(a) rejections above), but do not teach that the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Tseng teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038). Therefore, at the time of the invention, it would have been obvious to one Of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and taught by claim 6, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and Tseng (U.S. 2005/0035460) as applied to claims 11 and 17 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1).

Regarding claims 14 and 19, Chang, Lim, and Tseng together teach the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejection above).

Tseng additionally teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate the integrated circuit taught by Chang, Lim, and Tseng together, and also taught by claims 11 and 17, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Regarding claims 21, 22 and 24, Chang, Lin and Tseng fail to teach: claim 21 (new): The method as claimed in claim 1 wherein: forming the ultra-uniform silicide includes depositing the silicide metal using a vapor deposition process with a power level below 500 watts direct current. Claim 22 (new): The method as claimed in claim I wherein: forming the ultra-uniform silicide includes depositing the silicide metal at a deposition rate below approximately 7.0 Angstroms per second. Claim 24 (new): The method as claimed in claim 6 wherein: forming the ultra-uniform silicide includes

depositing the silicide metal at a deposition rate below approximately 7.0 Angstroms per second. In regards to the power and rate of deposition, these values would be determined through routine experimentation and would not lend themselves to patentability in the instant application without displaying unexpected results. See in Re Aller.

Response to Arguments

Applicant's arguments filed 3/13/09 have been fully considered but they are not persuasive. As noted in the Affirmed Decision of the BPAI mailed 6/20/08; We have thoroughly reviewed each of Appellants' arguments toward patentability. However, we find ourselves in complete agreement with the Examiner's reasoned analysis and application of the prior art, as well as her cogent and thorough disposition of the arguments raised by Appellants.

Accordingly, we will adopt the Examiner's reasoning as our own in sustaining the rejections of record, and we add the following for emphasis only. Chang, like Appellants, discloses a method of forming an integrated circuit comprising forming a gate dielectric on a semiconductor substrate, forming a gate on the gate dielectric, forming source/drain junctions in the semiconductor substrate, and forming a nickel silicide on the junctions at a temperature in the range of about 400-800°C. Since Appellants' Specification discloses that the thermal budget for forming the nickel silicide is in the Application/Control Number: 10/791,096 Page 13 Art Unit: 2829 range of about 400-450°C, the Examiner has properly concluded that it would have been obvious for one

with ordinary skill in the art to form the silicide layer of Chang with uniform the claimed thermal budget.

Although Chang discloses that the silicide layer may be formed at temperatures outside, as well as with uniform, Appellants' disclosed range, we find no merit in Appellants' argument that such is a teaching away from the claimed thermal budget. One of ordinary skill in the art would have found it obvious to operate at all the temperatures with uniform the range disclosed by Chang. Furthermore, we find that it would have been obvious for one with ordinary skill in the art to resort to routine experimentation to determine the optimum thermal budget for forming the claimed silicide and contact liners. Contrary to Appellants' argument regarding the criticality of the disclosed thermal budget, Appellants have proffered no objective evidence that the asserted criticality would have been truly unexpected to one of ordinary skill in the art. In reMerck & Co., 800 F.2d 1091, 1099 (Fed. Cir. 1986); In re Klosak, 455 F.2d 1077, 1080 (CCPA 1972). Indeed, Appellants acknowledge the following at page 3 of the Reply Brief:.

As well known to those skilled in the art and previously partially explained, the thermal budget defines the total amount of thermal energy transferred to the wafer during a given elevated temperature operation which is proportional to the temperature and duration of the process such that a low thermal budget is possible even at a very high temperature if the time of the process is short. For semiconductor processes, the thermal budget is generally given in units of °C. Exceeding the thermal budget will result in a defective or inoperative integrated circuit. Exceeding a temperature for a short

enough time would not affect the integrated circuit.

Consequently, Appellants' acknowledgement underscores that the claimed thermal budget was a known result effective variable for making a satisfactory integrated circuit, and it is well settled that the determination of the optimum value of a result effective variable is a matter of obviousness for one of ordinary skill in the art. In re Boesch, 617 F.2d 272, 276 (CCPA 1980).

Concerning the claimed step of depositing an interlayer dielectric having contact holes therein above the semiconductor substrate, Appellants have not rebutted the Examiner's reasoning that Lim supports the obviousness of forming such an interlayer dielectric above the semiconductor substrate of Chang by evidencing that it "well known in the art of semiconductor processing as a means of providing and accessing electrical signals to and from devices on an integrated circuit" (Arts. 17, second sentence). Appellants' argument that Chang does not disclose such an interlayer dielectric, and Lim does not disclose the formation of a silicide, is an ineffective attack on the references individually that fails to address the thrust of the Examiner's rejection based on the collective teachings of Chang and Lim.

Regarding the claimed ultra-uniform thickness of the nickel silicide, we fully concur with the Examiner that Tseng evidences the obviousness of forming an ultra-uniform nickel silicide of 50 Angstroms in order to obtain a semiconductor device with reduced contact resistance. We find no merit in Appellants' argument that Tseng's disclosure of a preference for a silicide thickness between about 50 Angstroms and 350 Angstroms is a teaching away of ultra-uniform silicides, in general, and silicides having

a thickness of about 50 Angstroms, in particular. Furthermore, the Examiner correctly notes that the claims on appeal do not recite a silicide thickness of 50 Angstroms, and Appellants' Specification fails to define a particular thickness for the claimed "ultra uniform thickness." The disclosure at page 7 of Appellants' Specification, cited by Appellants, defines an ultra-uniform silicide as having no variations in thickness greater than about 3 percent of the overall thickness and that it is preferable to achieve an ultra-uniform thickness of not more than 50 Angstroms. Such a stated preference does not define a value for the claimed ultra-uniform thickness and, furthermore, such a preference would seem to allay any suggestion of the criticality for the unspecified ultra-uniform thickness.

As a final point, we note that Appellants base no argument upon objective evidence of nonobviousness, such as unexpected results. Assertions of preferences or, for that matter, criticality in the Specification without supporting objective data is no substitute for factual evidence of unexpected results.

Furthermore: In regards to the ultra-uniform silicide as having no variations in thickness greater than about 3 percent of the overall thickness and that it is preferable to achieve an ultra-uniform thickness of not more than 50 Angstroms this would have been determined trough routine experimentation and would not lend itself to patentability in the instant application, without displaying unexpected results. (In re Aller)

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL S. LEBENTRITT whose telephone number is (571)272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael S.Lebentritt
Primary Examiner
Art Unit 2829

/Michael S. Lebentritt/

Primary Examiner, Art Unit 2829